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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,886	08/28/2003	Horng-Wen Chen	TSM6283131RI	8712

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EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,886	CHEN ET AL.	
	Examiner	Art Unit	
	George A. Goudreau	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *(8-28-03' to 10-27-03')*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-19* is/are allowed.

6)☒ Claim(s) *20, 22-24, 27-29, 31-37, 40, 43-45, 47-53, and 56* is/are rejected.

7)☒ Claim(s) *21,25,26,30,38,39,41,42,46,54,55,57 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

George A Goudreau

GEORGE GOUDREAU
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-19 are allowed.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 20, 22-24, 34-37, 40, 43-45, 47, 50-53, and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang et. al. (6,156,485).

Tang et. al. disclose a multi-step etching process for patterning an Al-Cu wiring layer on the surface of wafer which is comprised of the following steps:

Embodiment # 1:

-A photo-resist/PEOX/TiN/Al-Cu/TiN/SiO2 multi-layer laminate is formed onto the surface of a wafer.;

-The PEOX/TiN layers are etched using the patterned photo-resist etch mask, and a plasma, which is comprised of Cl2-BCl3-CF4.;

-The photo resist etch mask is removed using a O2 ashing process.; and

-The Al-Cu layer is etched using the PEOX/TiN layers as a hard mask, and a plasma, which is comprised of Cl2-BCl3.

Embodiment # 2:

-A photo-resist/BARC/W/TiN/Al-Cu/SiO2 multi-layer laminate is formed onto the surface of a wafer.;

-The BARC/W laminate are etched using a patterned photo resist etch mask, and a plasma, which is comprised of SF6-CF4-CHF3-N2.;

-The photo resist is removed using an O2 ashing process.;

-The BARC layer is removed.; and

-The Al-Cu layer is etched using a W hard mask, and a plasma, which is comprised of Cl2-BCl3.

The BARC layer may be comprised of any of an organic layer, SiON, or SiO2.

This is discussed in columns 1-10. This is shown in figures 1-4.

4. Claims 27, 31, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Keller (5,346,586).

Keller discloses a process for patterning a W polycide gate using a process comprised of the following steps:

-A photo resist/ SiO2 hard mask/ W polycide/ SiO2 laminate is formed on the surface of a Si wafer.;

-The photo resist is patterned, and used in the plasma etching of the SiO2 hard mask layer using a plasma which is comprised of (CF4-CHF3).;

-The WSi2 layer is plasma etched in a (SF6-He-O2) plasma using the patterned photo resist/ SiO2 hard mask as an etch mask.;

-The photo resist etch mask is removed from the wafer surface in-situ in the plasma etching chamber using an O3 based plasma.; and

The polysi layer is plasma etched using the SiO2 hard mask, and a plasma, which is comprised of (HBr-Cl2).

This is discussed specifically in columns 3-8; and discussed in general in columns 1-8. This is shown in figures 1-2.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 28-29, 32, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller as applied in paragraph 4 above further in view of Hills et. al. (5,382,316).

Keller as applied in paragraph 4 above fail to disclose the following aspects of applicant's claimed invention:

-the specific removal of the hard mask from the polysi layer after the polysi gate has been formed;

-the specific usage of a two-step plasma etching process for patterning the polysi layer;

-the specific usage of a plasma which is comprised of CF4 to remove the etch polymers from the SiO2 hard mask after the hard mask has been etched but prior to the etching of the polysi layer; and

-the specific usage of a hard mask made out of SiON

Hills et. al. teach that it is desirable to simultaneously remove a photo resist etch mask, and etch polymers left on a polysi gate which was patterned in a previous plasma etching step by employing a plasma which is comprised of (CF4-H2O-O2). This is discussed specifically in columns 2-3; and discussed in general in columns 1-6. This is shown in figures 1-2.

It would have been obvious to one skilled in the art to replace the O3 based plasma which was used to remove the photo-resist etch mask in the etching process taught above with a plasma which is comprised of (CF4-H2O-O2) based upon the teachings of Hills et. al. that this is a desirable means for removing both a photo resist etch mask as well as polymeric etch residues left on a wafer from a previous plasma-etching step. Further, this would have simply involved the usage of an alternative, and at least equivalent means for removing the photo resist etch mask to those means specifically taught by Keller. (In this instance, the photo resist stripping step, and the SiO2 hard mask-cleaning step would be comprised of the same process step since both processes occur at the same time simultaneously.)

It would have been obvious to one skilled in the art to replace the SiO2 hard mask employed in the etching process taught above with a SiON hard mask based upon the following. The usage of SiON as a hard mask in the patterning of a polysi gate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this would simply represent the usage of an alternative, and at least equivalent means for providing a hard mask to be used in the patterning of a polysi layer to those means, which are specifically taught above.

It would have been obvious to one skilled in the art to remove the hard mask after the polysi gate has been patterned in the etching process taught above based upon the following. The removal of a hard mask after it's usage in the patterning of a gate electrode is conventional or at least well known in the semiconductor processing arts. (The takes official notice in this regard.) Further, the hard mask would have had to been removed from the gate electrode after its formation in the process taught above in order to facilitate further processing of the wafer to form a device.

It would have been obvious to one skilled in the art to employ a two step plasma etching process to pattern the polysi layer in the etching process taught above based upon the following. The usage of a two-step plasma etching process to pattern a polysi gate electrode layer on a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this would have simply provided a means for reducing the amount of damage which is done to the SiO2 pad layer during

the polysi etching step without significantly impairing the overall etching speed of the polysi layer by providing a low selectivity, high etching rate, first etch step followed by a high selectivity, low etching rate, second, etch step for patterning the polysi layer on the SiO2 pad layer.

8. Claims 33, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied in paragraph 7 above further in view of Chapman (5,976,769).

The references as applied in paragraph 7 above fail to disclose the following aspects of applicant's claimed invention:

-the specific trimming of the width of the photo resist layer prior to using it to pattern the hard mask layer on the polysi layer

Chapman teaches that it is desirable to employ a plasma which is comprised of (O2-He) to trim the width of the patterned photo resist etch mask which is used to pattern a BARC layer in order to enhance the resolution of the etching process over that which is possible using prior art methods. The trimmed photo resist etch mask is then used in the anisotropic etching of a hard mask used to pattern a polysi layer on a wafer to form a polysi gate electrode. This is discussed specifically in columns 2-4, and discussed in general in columns 1-8. This is shown in figures 2 a – 2 h; and shown in general in figures 1-9.

It would have been obvious to one skilled in the art to trim the patterned photo resist etch mask after forming it but prior to using it to pattern the hard mask in the etching process taught above based upon the teachings of Chapman

that it is desirable to do so in order to enhance the resolution of a dry etching process.

9. Claims 21, 25-26, 30, 38-39, 41-42, 46, 54-55, and 57-58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number (571)-272-1434.

George A. Goudreau
Primary Examiner
Art Unit 1763